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Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attorney for Appellants

Date: 16 March 2004



image

AF 2800

**PATENT**
**Attorney Docket No.:** DB000575-012

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | | | |
|---|---|---|---|
| **Applicant(s):** | Keeth, et al. | ) | |
| | | ) | **Examiner:** Anh Quan Tra |
| **Serial No.:** | 09/885,217 | ) | |
| | | ) | **Art Unit:** 2816 |
| **Filed:** | 20 June 2001 | ) | |

**Entitled:** 256 MEG DYNAMIC RANDOM ACCESS MEMORY

## TRANSMITTAL

To: Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-captioned application, please find the following:

- Appellants' Brief Before the Board of Patent Appeals and Interferences (in triplicate);
- Fee Transmittal (PTO/SB/17); and
- Check in the amount of $330 as the requisite fee for filing the appeal brief.

Also enclosed is a return postcard. Please date stamp the postcard and return it to the address thereon in order to acknowledge receipt of the above-mentioned correspondence. The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to our Deposit Account No. 20-0888. A duplicate copy of this Transmittal letter is enclosed.

Respectfully submitted,

Edward L. Pencoske
Reg. No. 29,688
Thorp, Reed & Armstrong
One Oxford Centre, 14th Floor
Pittsburgh, PA 15219
(412) 394-7789
Attorney for Applicants

Dated: 16 March 2004

PTO/SB/17 (10-03)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



# FEE TRANSMITTAL for FY 2004

*Effective 10/01/2003. Patent fees are subject to annual revision.*

☐ Applicant claims small entity status. See 37 CFR 1.27

**TOTAL AMOUNT OF PAYMENT** ($) 330

| *Complete if Known* | |
|---|---|
| Application Number | 09/885,217 |
| Filing Date | 20 June 2001 |
| First Named Inventor | Keeth et al. |
| Examiner Name | Anh Quan Tra |
| Art Unit | 2816 |
| Attorney Docket No. | DB000575-012 |

## METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 20-0888

Deposit Account Name: Thorp Reed & Armstrong

**The Director is authorized to:** *(check all that apply)*

☐ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

## FEE CALCULATION

### 1. BASIC FILING FEE

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1001 | 770 | 2001 | 385 | Utility filing fee | |
| 1002 | 340 | 2002 | 170 | Design filing fee | |
| 1003 | 530 | 2003 | 265 | Plant filing fee | |
| 1004 | 770 | 2004 | 385 | Reissue filing fee | |
| 1005 | 160 | 2005 | 80 | Provisional filing fee | |

**SUBTOTAL (1)** ($) 0

### 2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

| | Extra Claims | | Fee from below | | Fee Paid |
|---|---|---|---|---|---|
| Total Claims | | -20** = | | X | = |
| Independent Claims | | - 3** = | | X | = |
| Multiple Dependent | | | | | = |

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description |
|---|---|---|---|---|
| 1202 | 18 | 2202 | 9 | Claims in excess of 20 |
| 1201 | 86 | 2201 | 43 | Independent claims in excess of 3 |
| 1203 | 290 | 2203 | 145 | Multiple dependent claim, if not paid |
| 1204 | 86 | 2204 | 43 | ** Reissue independent claims over original patent |
| 1205 | 18 | 2205 | 9 | ** Reissue claims in excess of 20 and over original patent |

**SUBTOTAL (2)** ($) 0

***or number previously paid, if greater; For Reissues, see above*

## FEE CALCULATION (continued)

### 3. ADDITIONAL FEES

| Large Entity Fee Code | Large Entity Fee ($) | Small Entity Fee Code | Small Entity Fee ($) | Fee Description | Fee Paid |
|---|---|---|---|---|---|
| 1051 | 130 | 2051 | 65 | Surcharge - late filing fee or oath | |
| 1052 | 50 | 2052 | 25 | Surcharge - late provisional filing fee or cover sheet | |
| 1053 | 130 | 1053 | 130 | Non-English specification | |
| 1812 | 2,520 | 1812 | 2,520 | For filing a request for *ex parte* reexamination | |
| 1804 | 920* | 1804 | 920* | Requesting publication of SIR prior to Examiner action | |
| 1805 | 1,840* | 1805 | 1,840* | Requesting publication of SIR after Examiner action | |
| 1251 | 110 | 2251 | 55 | Extension for reply within first month | |
| 1252 | 420 | 2252 | 210 | Extension for reply within second month | |
| 1253 | 950 | 2253 | 475 | Extension for reply within third month | |
| 1254 | 1,480 | 2254 | 740 | Extension for reply within fourth month | |
| 1255 | 2,010 | 2255 | 1,005 | Extension for reply within fifth month | |
| 1401 | 330 | 2401 | 165 | Notice of Appeal | |
| 1402 | 330 | 2402 | 165 | Filing a brief in support of an appeal | 330 |
| 1403 | 290 | 2403 | 145 | Request for oral hearing | |
| 1451 | 1,510 | 1451 | 1,510 | Petition to institute a public use proceeding | |
| 1452 | 110 | 2452 | 55 | Petition to revive - unavoidable | |
| 1453 | 1,330 | 2453 | 665 | Petition to revive - unintentional | |
| 1501 | 1,330 | 2501 | 665 | Utility issue fee (or reissue) | |
| 1502 | 480 | 2502 | 240 | Design issue fee | |
| 1503 | 640 | 2503 | 320 | Plant issue fee | |
| 1460 | 130 | 1460 | 130 | Petitions to the Commissioner | |
| 1807 | 50 | 1807 | 50 | Processing fee under 37 CFR 1.17(q) | |
| 1806 | 180 | 1806 | 180 | Submission of Information Disclosure Stmt | |
| 8021 | 40 | 8021 | 40 | Recording each patent assignment per property (times number of properties) | |
| 1809 | 770 | 2809 | 385 | Filing a submission after final rejection (37 CFR 1.129(a)) | |
| 1810 | 770 | 2810 | 385 | For each additional invention to be examined (37 CFR 1.129(b)) | |
| 1801 | 770 | 2801 | 385 | Request for Continued Examination (RCE) | |
| 1802 | 900 | 1802 | 900 | Request for expedited examination of a design application | |

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

**SUBTOTAL (3)** ($) 330

| SUBMITTED BY | | | | (Complete *(if applicable)*) | |
|---|---|---|---|---|---|
| *Name (Print/Type)* | Edward L. Pencoske | *Registration No. (Attorney/Agent)* | 29,688 | *Telephone* | 412-394-7789 |
| *Signature* | E L Pencoske | | | *Date* | 16 March 2004 |

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:

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Attorney for Appellants

Date: 16 March 2004

**Appl. No.:** 09/885,217
**Applicant(s):** Keeth, et al.
**Filed:** 20 June 2001
**Title:** 256 MEG DYNAMIC RANDOM ACCESS MEMORY

**Art Unit:** 2816
**Examiner:** Anh Quan Tra

**Docket No.:** DB000575-012

## APPELLANTS' BRIEF BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

(1) *Real Party In Interest*

The real party in interest in this case is Micron Technology, Inc. the assignee of the entire interest of the above-identified patent application.

(2) *Related Appeals and Interferences*

There are no known appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the instant case.

This application is a divisional of U.S. Patent Application No. 09/620,606 filed 20 July 2000, which issued on 4 June 2002 as U.S. Patent No. 6,400,595, which is a divisional application of U.S. Application No. 08/916,692 filed 22 August 1997, which issued on 6 November 2001 as U.S. Patent No. 6,314,011 and claims the benefit of U.S. Provisional Patent No. 60/050,929 filed 30 May 1997.

(3) *Status of the Claims*

The status of the claims remains as set forth in the Final Office Action dated 13 November 2003. Specifically, claims 223, 225 – 237, 247 – 250, 496, and 499 – 515 are pending. Claims 223 and 511 are rejected pursuant to 35 U.S.C. §102 (e) and claims 225, 228 – 237, 247 – 250, 496, 499 – 510, and 512 – 515 are rejected pursuant to 35 U.S.C. §103(a). Claims 226 and 227 are objected to. Claims 223, 225 – 237, 247 – 250, 496, and 499 – 515 are on appeal.

(4) *Status of Amendments*

A Response and Amendment was filed on 24 September 2003 in response to an Office action mailed 10 September 2003. A Final Office action was mailed 13 November 2003 in which the Examiner considered the arguments submitted in the Response and Amendment but maintained the rejections set forth in the 10 September Office action. No amendments have been filed subsequent to the 13 November 2003 Final Office action.

(5) *Summary of Invention*

The patent application discloses an apparatus and method for generating a reference voltage for a dynamic random access memory. Reference numbers in the following discussion refer to the structures shown in FIGS. 35, 36A1, 36A2, 36A3, and 36B[1].

A voltage regulator 220 is provided for producing a peripheral voltage ($V_{CC}$, $V_{CCA}$) which is related to (for example as illustrated in FIG. 36B) an external voltage ($V_{CCX}$). As shown in FIG. 35, the voltage regulator includes a control circuit 226, a voltage reference circuit 224, and an amplifier portion 222.

The voltage reference circuit 224 is responsive to the external voltage ($V_{CCX}$) and produces a reference voltage ($V_{ref}$). (See FIG. 36A1 – 36A3.) The voltage reference circuit is comprised of an active reference circuit which receives the external voltage ($V_{CCX}$) and produces a reference signal (at node 232) having the desired relationship with the external voltage ($V_{CCX}$). (See FIGS. 36A1 – 36A3; page 95, lines 14 – 18.) The active reference circuit may be comprised of a current source 228 which provides current to a diode stack 234. (See page 14, lines 10 – 16.) The diode stack 234 may have an adjustable impedance. (See page 94, lines 16 – 20.) The voltage reference circuit 224 also includes a unity gain amplifier 238. (See FIG. 36A1 – 36 A3.) The unity gain amplifier 238, in response to the reference signal (at node 232), produces the reference voltage ($V_{ref}$) which is made available at the output terminal 240. (See page 95, line 25 to page 96, line 3.)

The reference voltage ($V_{ref}$) produced by the voltage reference circuit 224 is input into the amplifier portion 222. (See FIG. 35; page 93, lines 23- 26.) The amplifier portion 222 amplifies the reference voltage ($V_{ref}$) produced by the voltage reference circuit 224 by a factor greater than unity to provide an output voltage ($V_{CC}$). (See FIG. 35; page 101, line 22 to page 102, line 4.)

Additionally, the present invention is directed to a method of supplying an output voltage ($V_{CC}$) in response to an external voltage ($V_{CCX}$), wherein the output voltage has a first characteristic when the external voltage is in a powerup range, has a second characteristic when the external voltage is in an

[1] A copy of FIGS. 35, 36A1 – 36A3, and 36B are found in Exhibit A; FIGS. 36A1 – 36A3 have been combined to form a single drawing for the Board's convenience. Pages 92 through 99 of the specification are found in Exhibit B.

operating range, and has a third characteristic when the external voltage is in a burn-in range. (See FIG. 36B.) When the external voltage is below a first predetermined value (i.e., in the powerup range), the external voltage ($V_{CCX}$) is supplied as the output voltage ($V_{CC}$). (See FIG. 36B, region 1.) When the external voltage ($V_{CCX}$) is above the first predetermined value (i.e., in the operating range), a reference signal (at node 232) having a desired relationship with the external voltage ($V_{CCX}$) is produced; the reference signal (at node 232) is amplified with a unity gain amplifier 238 to produce a reference voltage ($V_{ref}$). (See FIG. 36B, region 2.) When the external voltage ($V_{CCX}$) is above a second predetermined value (i.e., in the burn-in range), the reference voltage ($V_{ref}$) is amplified by a factor greater than unity to provide the output voltage ($V_{CC}$). (See FIG. 36B, region 3; see also page 94 line 3 to page 99, line 17.)

(6) *Issues*

(a) Whether independent claim 223 is anticipated by Morishita et al. pursuant to 35 U.S.C. §102 (e). More specifically, does Morishita disclose "a unity gain amplifier responsive to said reference signal [produced by an active reference circuit] for producing the reference voltage"?

(b) Do any of the secondary references (Zarrabian used in a rejection of independent claim 496; Tsay used in a rejection of independent claims 231 and 504; and Hayakawa and Park used in a rejection of independent claim 247) provide the missing teachings?

(7) *Grouping of Claims*

An argument is provided demonstrating the patentability of claim 223 over Morishita et al. All of the remaining claims on appeal, claims 225 – 237, 247 – 250, 496, and 499 – 515, stand or fall with claim 223.

(8) *Argument*

(a) *Morishita et al. does not disclose "a unity gain amplifier responsive to said reference signal [produced by an active reference circuit] for producing the reference voltage."*

Claim 223 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Morishita et al. (US Pat. No.: 5,757,175). Specifically, the Examiner states:

> As to claim 223, Morishita et al. discloses in figures 17 and 19 a voltage reference circuit responsive to an external voltage ($ExtV_{CC}$) for supplying a reference voltage ($INV_{CC}$), comprising: an active reference circuit (VGR, figure 19) for receiving the external voltage and for producing a reference signal ($V_{ref}$) having a desired relationship with the external voltage, the active reference circuit comprising a current source (TP4) utilizing a current mirror for providing current to a diode stack (CVC) having an adjustable impedance, wherein the reference signal is dependent upon the external voltage (column 2, lines 17-20, teaches that the reference voltage $V_{ref}$ is independent of the external power supply voltage $EXV_{CC}$ when the voltage $EXV_{CC}$ is <u>at least at a prescribed voltage level</u>. [Emphasis in original.] Thus, when the voltage $EXV_{CC}$ is lower than the prescribed voltage level, the reference voltage is dependent of the external supply voltage $EXV_{CC}$);

and a unity gain amplifier (CMP, DT) responsive to the reference signal for producing the reference voltage.

Claim 223 recites "an active reference circuit ... for producing a reference signal ..." and "a unity gain amplifier responsive to said reference signal for producing the reference voltage." It is respectfully submitted that the unity gain amplifier of the claimed voltage reference circuit produces the reference voltage $V_{ref}$. Referring to FIGS. 36A1 – 36A3, the active reference circuit uses a current source 228 and a diode stack 234 to produce a reference signal at circuit node 232. (See specification, page 94, line 3 to page 95, line 24.) The reference signal is then input into the unity gain amplifier 238. (See specification, page 95, lines 25 – 26.) The output of the unity gain amplifier is the reference voltage $V_{ref}$. As stated in the specification, "the output of the unity gain amplifier 238 is available at the output terminal 240." (See page 95, line 26 to page 96, line 3.) By using the unity gain amplifier as a component of the claimed voltage reference circuit, "common mode range and overall voltage characteristics are improved." (See page 96, lines 7 – 9.) The regulated reference voltage $V_{ref}$ may then be input into an amplifier portion 222 to produce an array voltage $V_{CCA}$ and peripheral voltage $V_{CC}$ among others. (See FIG. 35, and page 96, lines 23 – 26.)

In contrast, Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal. As best illustrated in figure 17, the reference voltage $V_{ref}$ is produced by the reference voltage generating circuit VRG. (See also column 1, line 66 to column 2, line 5.) Figure 19 illustrates a detailed view of the reference voltage generating circuit VRG shown in Figure 17. The reference voltage generating circuit VRG does not include a unity gain amplifier as a component thereof.

The Examiner states that the comparator CMP and driver transistor DT comprise "a unity gain amplifier responsive to the reference signal for producing the reference voltage." It is respectfully submitted that the Examiner has misconstrued the teachings of Morishita. Morishita discloses that the comparator CMP is used to compare the reference voltage $V_{ref}$, which is produced solely by the reference voltage generating circuit VRG, to the internal power supply voltage INVcc carried on the internal power supply line PSL. (Column 2, lines 5 – 9.) Morishita states:

> Comparator CMP reduces its output signal level if the internal power supply voltage $INV_{CC}$ is lower than the reference voltage $V_{ref}$, while it outputs a signal at an H level when the internal power supply voltage $INV_{CC}$ is higher than the reference voltage $V_{ref}$. Driver transistor DT has its conductance increased with reduction in potential level of the output signal of comparator CMP, to supply large current. Meanwhile, the driver transistor DT has its conductance reduced with the internal power supply voltage $INV_{CC}$ being higher than the reference voltage $V_{ref}$, to stop current supply onto internal power supply line PSL. This internal power supply down-converter therefore maintains the internal power supply voltage $INV_{CC}$ at the reference voltage $V_{ref}$ level.

(Column 2, lines 21 – 34.) Accordingly, Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier for producing a reference voltage in response to a reference signal.

Thus, for the reasons discussed above, it is believed that claim 223 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 223 pursuant to §102(e) in view of Morishita be withdrawn.

(b) *None of the secondary references provides the missing teachings of Morishita.*

(1) *Claim 496*

Claim 496 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over Morishita in view of Zarrabian (US Pat. No.: 5,838,076). Claim 496 recites "a unity gain amplifier responsive to a signal available at the node for producing the reference voltage." As discussed above, it is believed that Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal. It is respectfully submitted that the Office has not demonstrated that Zarrabian provides this missing teaching. Thus, for the same reasons discussed above in conjunction with claim 223, it is believed that claim 496 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 496 be withdrawn.

(2) *Claims 231 and 504*

Claims 231 and 504 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Tsay et al (US Pat. No.: 6,127,881) in view of Morishita. As to claims 231 and 504, the Examiner stated:

> Tsay's figure 2 shows a multiplier circuit for generating a voltage signal higher than a reference voltage ($V_{ref}$). Thus, Tsay's figure 2 shows all limitations of the claims except for detail of the reference circuit. [Emphasis added]

Claim 231 recites "a unity gain amplifier responsive to said reference signal for producing a reference voltage." Claim 504 recites "a unity gain amplifier responsive to a signal available at the node for producing a reference voltage." As discussed above in conjunction with claims 223 and 496, Morishita fails to teach a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal and, as stated by the Examiner, Tsay fails to provide this missing teaching. Thus, it is believed that claims 231 and 504 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 231 and 504 be withdrawn.

(3) *Claim 247*

Claim 247 stands rejected under 35 U.S.C. §103 (a) as being unpatentable over Hayakawa in view of Tsay, Morishita and Park. Claim 247 recites "amplifying the reference signal with a unity gain amplifier for producing a reference voltage when the external voltage is above said first predetermined value." As discussed above, Tsay and Morishita fail to suggest or teach a voltage reference circuit that includes a unity gain amplifier that produces a reference voltage in response to a reference signal and the

Office has not demonstrated that Park or Hayakawa provide the missing teachings. Thus for the same reasons discussed above, it is believed that claim 247 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 247 be withdrawn.

*Conclusion*

For the reasons set forth above appellant respectfully requests that the rejections of independent claims 223, 231, 247, 496, and 504 be withdrawn and the application be allowed to issue with all of the pending claims, 223, 225 – 237, 247 – 250, 496, and 499 – 515.

Respectfully Submitted,

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(412) 394-7789
Attorney for Appellants

Dated : 16 March 2004

(9) Appendix – Claims on Appeal

Claim 223

A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage, said active reference circuit comprising a current source utilizing a current mirror for providing current to a diode stack having an adjustable impedance, wherein said reference signal is dependent upon said external voltage; and

a unity gain amplifier responsive to said reference signal for producing the reference voltage.

Claim 225

The voltage reference circuit of claim 223 wherein said diode stack includes a plurality of transistors connected in series, with each transistor's gate connected to a common potential, and a plurality of switches each for selectively shunting one of said transistors.

Claim 226

The voltage reference circuit of claim 225 wherein said switches are controlled by fuses, and wherein opening certain of said fuses turns its associated switch on, and wherein opening certain other of said fuses turns its associated switch off.

Claim 227

The voltage reference circuit of claim 226 wherein said plurality of transistors includes a first plurality of field effect transistors and wherein said plurality of switches includes a second plurality of field effect transistors.

Claim 228

The voltage reference circuit of claim 223 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value.

Claim 229

The voltage reference circuit of claim 228 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 230

The voltage reference circuit of claim 229 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 231

A voltage reference circuit in combination with a power amplifier, said combination comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship to the external voltage, wherein said reference signal is dependent upon said external voltage;

a unity gain amplifier responsive to said reference signal for producing a reference voltage; and

a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide an output voltage.

Claim 232

The combination of claim 231 additionally comprising a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value.

Claim 233

The combination of claim 232 wherein said circuit for supplying includes a switch for shorting a bus carrying the external voltage with a bus carrying the output voltage.

Claim 234

The combination of claim 232 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a second predetermined value.

Claim 235

The combination of claim 234 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 236

The combination of claim 235 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 237

The combination of claim 234 wherein said combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range, increases at a second slope substantially less than a slope of the external voltage during an operating range, and increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage.

Claim 247

A method of supplying an output voltage in response to an external voltage, and wherein the output voltage has a first characteristic when the external voltage is in a powerup range, has a second characteristic when the external voltage is in an operating range, and has a third characteristic when the external voltage is in a burn-in range, said method comprising the steps of:

supplying the external voltage as the output voltage when the external voltage is below a first predetermined value defining the powerup range;

producing a reference signal having a desired relationship with the external voltage, wherein said reference signal is dependent upon said external voltage;

amplifying the reference signal with a unity gain amplifier for producing a reference voltage when the external voltage is above said first predetermined value;

amplifying the reference voltage by a factor greater than unity to provide the output voltage when the external voltage is not being supplied as the output voltage; and

pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds said second predetermined value defining the burn-in range.

Claim 248

The method of claim 247 wherein said step of producing a reference signal includes the steps of generating a current related to the external voltage, applying the current to a circuit node, and draining the current from the circuit node through an adjustable impedance.

Claim 249

The method of claim 248 additionally comprising the step of adjusting the impedance to modify the reference signal.

Claim 250

The method of claim 249 wherein said step of adjusting the impedance includes the step of opening a fuse.

Claim 496

A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

a constant current source for supplying a current to a node in response to the external voltage;

a circuit having an adjustable impedance for draining current from the node, wherein said circuit comprises a diode stack comprised of a plurality of transistors connected in series and a plurality of switches each switch for selectively shunting one of said transistors, and wherein each switch is responsive to a control signal; and

a unity gain amplifier responsive to a signal available at the node for producing the reference voltage, wherein said signal is dependent upon said external voltage.

Claim 499

The voltage reference circuit of claim 496 wherein said switches are controlled by fuses.

Claim 500

The voltage reference circuit of claim 499 wherein said plurality of transistors includes a first plurality of field effect transistors and wherein said plurality of switches includes a second plurality of field effect transistors.

Claim 501

The voltage reference circuit of claim 496 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value.

Claim 502

The voltage reference circuit of claim 501 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 503

The voltage reference circuit of claim 502 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 504

A voltage reference circuit in combination with a power amplifier, said combination comprising:

a constant current source for supplying a current to a node in response to an external voltage;

a circuit having an adjustable impedance for draining current from the node;

a unity gain amplifier responsive to a signal available at the node for producing a reference voltage, wherein said signal is dependent upon said external voltage; and

a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide an output voltage.

Claim 505

The combination of claim 504 additionally comprising a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value.

Claim 506

The combination of claim 505 wherein said circuit for supplying includes a switch for shorting a bus carrying the external voltage with a bus carrying the output voltage.

Claim 507

The combination of claim 505 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a second predetermined value.

Claim 508

The combination of claim 507 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 509

The combination of claim 508 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 510

The combination of claim 507 wherein said combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range, increases at a second slope substantially less than a slope of the external voltage during an operating range, and increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage.

Claim 511

The voltage reference circuit of claim 223 wherein said reference signal is dependent upon said external voltage within a predetermined testing margin of error.

Claim 512

The voltage reference circuit of claim 231 wherein said reference signal is dependent upon said external voltage within a predetermined testing margin of error.

Claim 513

The voltage reference circuit of claim 247 wherein said reference signal is dependent upon said external voltage within a predetermined testing margin of error.

Claim 514

The voltage reference circuit of claim 496 wherein said reference signal is dependent upon said external voltage within a predetermined testing margin of error.

Claim 515

The voltage reference circuit of claim 504 wherein said reference signal is dependent upon said external voltage within a predetermined testing margin of error.

EXHIBIT A



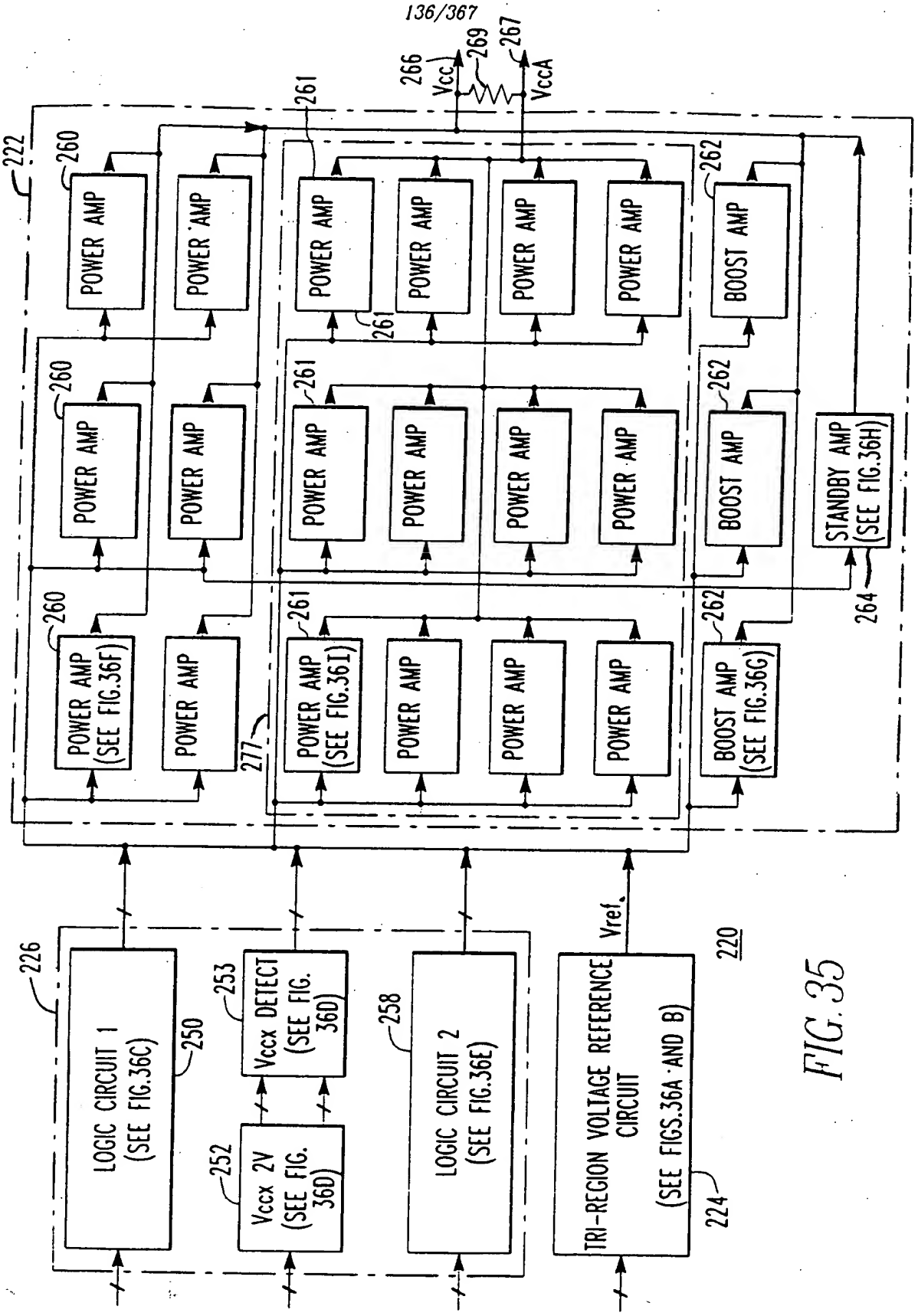



FIG. 35

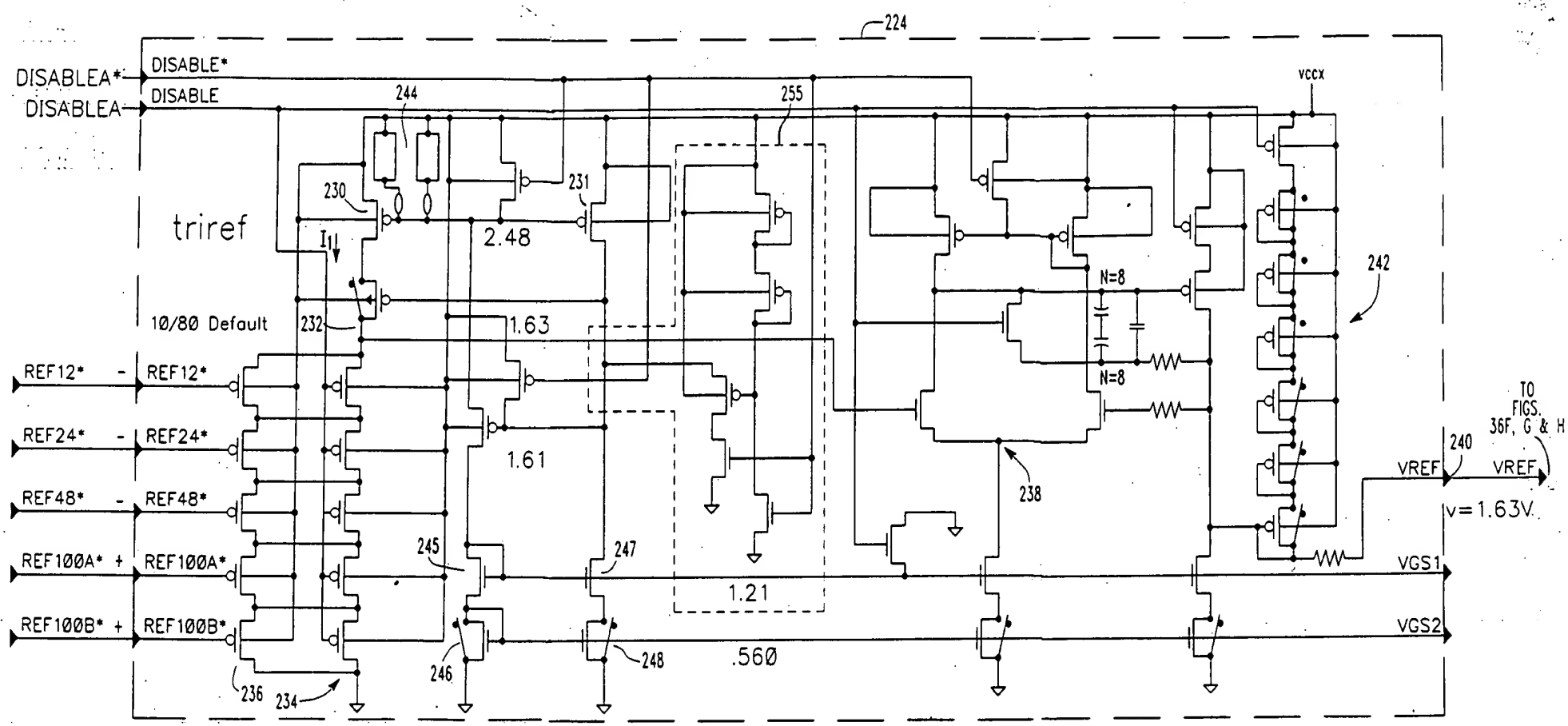



FIG. 36A1 FIG. 36A2 FIG. 36A3

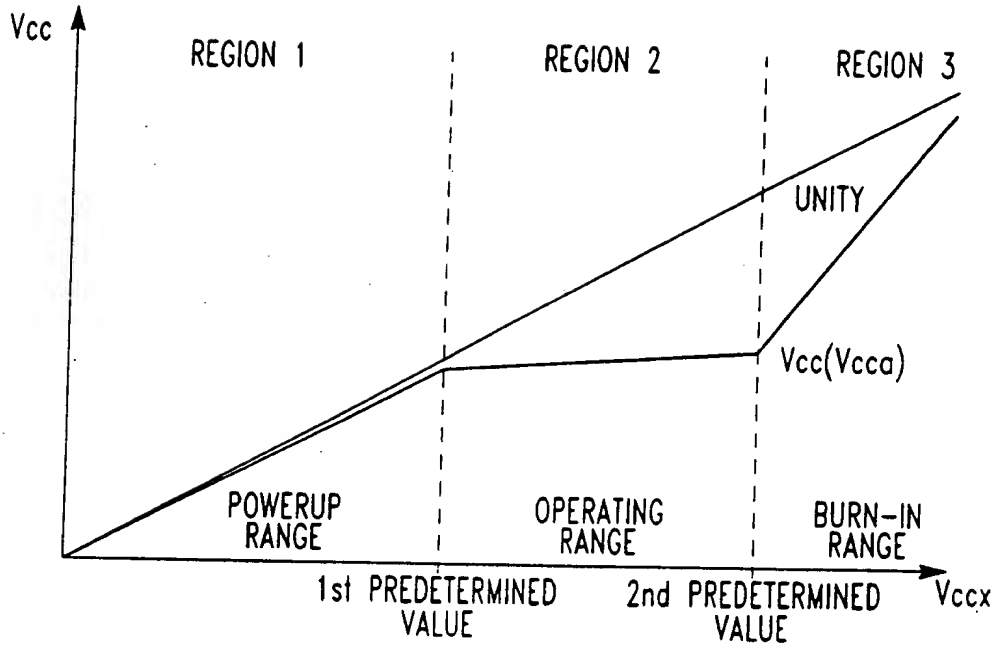
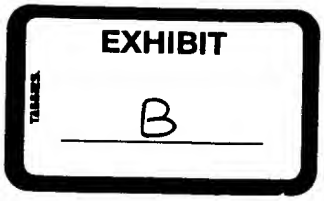



FIG. 36B




VII. Voltage Supplies

The chip 10 of the present invention produces from the externally supplied voltage Vccx all of the various voltages that are used throughout the chip 10. The voltage regulator 220 (FIG. 35) may be used to produce the array voltage Vcca and the peripheral voltage Vcc. The voltage pump 280 (FIG. 37) may be used to produce a back bias voltage Vbb for the die. The voltage pump 400 (FIG. 39) may be used to produce a boosted voltage Vccp needed for, inter alia, driving the word lines. The DVC2 generators 500-507 (FIG. 41) may be used to produce a bias voltage DVC2 for biasing the digitlines and a voltage AVC2 (which is equal to DVC2) for the cellplate. The voltage regulator, Vbb pump, Vccp pump, and DVC2 generators, which may be collectively referred to as a power supply, will each be described in detail.

FIG. 35 is a block diagram illustrating the voltage regulator 220 which may be used to produce the peripheral voltage Vcc and array voltage Vcca from the externally supplied voltage Vccx. As seen from FIG. 33E, the voltage regulator 220 is located in the center of the pads area 200 in what is referred to hereinbelow as the center logic (See Section VIII).

The process used to fabricate the chip 10 determines such properties as gate oxide thickness, field device characteristics, and diffused junction properties. Each of those properties in turn effects breakdown voltages and

leakage parameters which limit the maximum operating voltage which a part produced by a particular process can reliably tolerate. For example, a 16 Meg DRAM built on a 0.35 $\mu$m CMOS process with 120 angstrom gate oxide can operate reliably with an internal supply voltage not exceeding 3.6 volts. If that DRAM had to operate in a 5 volt system, an internal voltage regulator would be needed to convert the external 5 volt supply to an internal 3.3 volt supply. For the same DRAM operating in a 3.3 volt system, an internal voltage regulator would not be required. Although the actual operating voltage is determined by process considerations and reliability studies, the internal supply voltage is generally proportional to the minimum feature size. The following table summarizes that relationship.

Table 7

| Process | Vcc Internal |
|---|---|
| 0.45$\mu$M | 4.0 Volts |
| 0.35$\mu$M | 3.3 Volts |
| 0.25$\mu$M | 2.5 Volts |
| 0.20$\mu$M | 2.0 Volts |

The circuit 220 is comprised of three major sections, an amplifier portion 222, a tri-region voltage reference circuit 224, which produces a reference voltage input to the amplifier portion 222, and a control circuit 226 which

produces control signals input to the amplifier portion 222. Each will now be described in detail.

In FIG. 36A, the tri-region voltage reference circuit 224 is illustrated in detail. The tri-region voltage reference circuit 224 is comprised of a current source 228. A current I1 flowing through a resistor 244 generates a voltage which is equal to the gate to source voltage of a transistor 230. The drain to source voltage of another transistor 231 is equal to the gate to source voltage plus Vth. The current flowing through the transistor 231 is constrained by a current mirror comprised of transistors 245, 246, 247, and 248 to be equal to the current I1. In that manner, the current source 228 provides a current I1 to a circuit node 232. Current is drained from the circuit node 232 by a trimmable, or programmable, "pseudo" diode stack 234. The pseudo diode stack 234 is a plurality of transistors connected in series with their gate terminals connected to a common potential. The pseudo diode stack 234 is essentially a long channel FET which can be programmed or trimmed to provide the desired impedance.

Connected across each of the transistors in the pseudo diode stack 234 is a switching or trimming transistor from a stack 236 of such transistors. The gates of each of the switching transistors in the stack 236 are connected to a reference potential through a closed fuse or other type of device which may be either opened or closed. Assuming fuses

are used, half of the gates may be connected to a potential which renders the switching transistor conductive, thereby removing the associated transistor from the stack 234 while the gates of the remaining transistors may be connected through fuses to a potential which renders the switching transistor nonconductive, thereby leaving the associated transistor in the stack 234. In that manner, fuses may be blown to either turn on or turn off a switching transistor to thereby decrease or increase, respectively, the impedance of the trimmable diode stack 234. In that manner, a reference signal (voltage) available at the circuit node 232 can be precisely controlled. Such trimming is required due to process variations during fabrication.

The current source 228 together with the pseudo diode stack 234 and switching transistors 236 form an active voltage reference circuit which produces the reference signal available at the circuit node 232 that is responsive to the external voltage Vccx applied to the circuit 224. Those components are considered to form an active voltage reference circuit as contrasted with a resistor/trimmable pseudo diode stack combination found in the prior art which passively produces a signal at node 232. A bootstrap circuit 255 is also provided to "kickstart" the current source 228.

The reference signal available at circuit node 232 is input to a unity gain amplifier 238. The output of the

unity gain amplifier 238 is available at an output terminal 240 at which a regulated reference voltage Vref is available. Use of an active voltage reference circuit for producing the reference signal at circuit node 232 produces the desired relationship between Vref and Vccx which is not available with prior art circuits at the voltage range. Additionally, by making amplifier 238 a unity gain amplifier, common mode range and overall voltage characteristics are improved.

The tri-region voltage reference circuit includes a pullup stage 242 for pulling up the reference voltage available at output terminal 240 so that the reference voltage substantially tracks the external voltage when the external voltage exceeds a predetermined value. The pullup stage 242 is comprised of a plurality of diodes formed by pMOS transistors connected between the external voltage Vccx and the output terminal 240. When the voltage Vccx exceeds the voltage at the terminal 240 by the number of diode drops in the series connected diodes comprising the pullup stage 242, the pMOS diodes will be turned on clamping the voltage available at the output terminal 240 to Vccx minus the voltage drop across the diode stack.

The voltage available at the output terminal 240 is input to the amplifier portion 222 of the voltage regulator 220 where it is amplified to produce both the array voltage Vcca and peripheral voltage Vcc as will be described

hereinbelow in conjunction with a description of amplifier portion 222.

The relationship between the peripheral voltage Vcc and the externally supplied voltage Vccx is illustrated in FIG. 36B. The tri-region voltage reference circuit 224 is responsible for those portions of the curve occurring in region 2, corresponding to the "operating range" of the externally supplied voltage Vccx, and region 3, corresponding to the "burn-in range" of the externally supplied voltage Vccx. The output of the tri-region voltage reference circuit 224 is not used to generate the peripheral voltage Vcc during region 1. Region 1 is implemented by shorting the bus carrying the external voltage Vccx and the bus carrying the peripheral voltage Vcc together though pMOS output transistors found in the power stage of each power amplifier as will be described hereinbelow. The first region occurs during a powerup or powerdown cycle in which the externally supplied voltage Vccx is below a first predetermined value. In the first region, the peripheral voltage Vcc is set equal to the externally supplied voltage Vccx to provide the maximum operating voltage allowable in the part. A maximum voltage is desirable in region 1 to extend the DRAM's operating range and to ensure data retention during low-voltage conditions.

After the first predetermined value for the externally supplied voltage Vccx has been reached, the buses carrying

the voltages Vccx and Vcc are no longer shorted together. After the first predetermined value for the externally supplied voltage Vccx is reached, the normal operating range, region 2, illustrated in FIG. 36B is entered. In region 2, the peripheral voltage Vcc flattens out and establishes a relatively constant supply voltage to the peripheral devices of the chip 10. Certain manufacturers strive to make region 2 absolutely flat, thereby eliminating any dependance on the externally supplied voltage Vccx. A moderate amount of slope in region 2 is advantageous for characterizing performance. It is important in the manufacturing environment that each DRAM meet the advertized specifications with some margin for error. A simple way to ensure such margins is to exceed the operating range by a fixed amount during component testing. The voltage slope depicted in FIG. 36B allows that margin testing to occur by establishing a moderate degree of dependance between the externally supplied voltage Vccx and the peripheral voltage Vcc.

The third region illustrated in FIG. 36B is used for component burn-in, and is entered whenever the externally supplied voltage Vccx exceeds a second predetermined value. That second predetermined value is set by the number of diodes in the diode stack comprising pullup stage 242. During burn-in, both temperature and voltage are elevated above the normal operating range to stress the DRAM and weed

out infant failures. Again, if there were no relationship between the external voltage Vccx and the peripheral voltage Vcc, the internal voltage could not be elevated.

The characteristic of the peripheral voltage Vcc may be summarized as follows: the slope of the peripheral voltage Vcc is substantially the same as the slope of the external voltage Vccx in region 1 (up to the first predetermined value); the slope of the peripheral voltage Vcc is substantially less than the slope of the external voltage Vccx in region 2 (between the first predetermined value and the second predetermined value); and the slope of the peripheral voltage Vcc is greater than the slope of the external voltage Vccx in region 3 (above the second predetermined value) because the signal available at output terminal 240, which substantially tracks the external voltage Vccx, is multiplied in an amplifier having a gain greater than one.

The next section of the voltage regulator 220 is the control circuit 226. The control circuit 226 is comprised of a logic circuit 1 250 illustrated in FIG. 36C, a Vccx 2v circuit 252 and a Vccx detect circuit 253 illustrated in FIG. 36D, and a second logic circuit 258 illustrated in FIG. 36E. Turning first to FIG. 36C, the logic circuit 1 250 receives a number of input signals: SEL32M<0:7>, LLOW, EQ*, RL*, 8KREF, ACT, DISABLEA, DISABLEA*, and PWRUP. The logic circuit 1 250 may be comprised primarily of static CMOS